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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/939,636	08/28/2001	Kevin M. Devereaux	M4065.0477/P477	4394

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EXAMINER
NGUYEN, JOSEPH H

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 08/29/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/939,636	DEVEREAUX, KEVIN M.	
	Examiner	Art Unit	
	Joseph Nguyen	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 June 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) *12-24* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of claims 1-11 in Paper No. 5 is acknowledged. Therefore, claims 1-11 are hereby prosecuted whereas claims 12-24 are withdrawn from consideration.

Claim Objections

Claims 1 and 5 are objected to because of the following informalities: "a" in line 8 of claim 1 and "a" in line 1 of claim 6 should be removed. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 9 –11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 9 recites the limitation "the standard Vcc bonding pad" in 5. There is insufficient antecedent basis for this limitation in the claim.

Claim 10 recites the limitation "the standard Vss bonding pad" in 4. There is insufficient antecedent basis for this limitation in the claim.

Claim 11 is also rejected due to its dependency upon the rejected claim 9.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Green et al.

Regarding claim 1, Green et al discloses on figures 2 and 3 a semiconductor wafer 10 comprising at least one first sacrificial conductive line 24 for supplying a first voltage to a plurality of dies 12 fabricated on said wafer; a plurality of integrated circuit dies 12 fabricated on said wafer, each die comprising a first terminal 34 coupled to the circuitry within said die for supplying a first voltage to said circuitry; a second terminal 36 for supplying said first voltage to said first terminal; a voltage interruption device 42 provided between said first and second terminals interrupting an electrical coupling between said first and second terminals; and a first sacrificial terminal 40 for receiving said first voltage from said first sacrificial conductive line and supplying said first voltage to said second terminal.

Regarding claim 2, Green et al discloses on figures 2 and 3 each die 12 further comprises a first on die sacrificial conductive line (readable on figure 3, the line between 36 and 40) provided between the first sacrificial terminal 40 and second terminal 36.

Regarding claim 3, Green et al discloses on figures 2 and 3 the wafer further comprises at least one second sacrificial conductive line 28 for supplying a second

voltage to said plurality of dies 12; each die 12 further comprising a third terminal 32 coupled to the circuitry within said die for supplying a second voltage to said circuitry; and a second sacrificial terminal 38 for receiving said second voltage from said sacrificial second conductive line and supplying said second voltage to said third terminal.

Regarding claim 4, Green et al discloses on figures 2 and 3 each die 12 further comprises a second one die sacrificial conductive line (readable on figure 3, the line between 38 and 32) provided between the second sacrificial terminal 38 and third terminal 32.

Regarding claim 5, Green et al discloses on figures 2 and 3 the voltage interruption device 42 is a fuse.

Regarding claim 6, Green et al discloses on figures 2 and 3 the fuse 42 is blown when said die draws current in excess of a predetermined value.

Regarding claim 7, Green et al discloses on figures 2 and 3 further comprises a passivation layer having respective openings to the first and second sacrificial terminals, said first and second sacrificial terminals respectively connecting with said first and second sacrificial conductive lines through said openings (col. 4, lines 43-50).

Regarding claim 8, Green et al discloses on figures 2 and 3 comprises a first on die sacrificial conductive line (readable on figure 3) provided between the first sacrificial terminal and second terminal; and a second on die sacrificial conductive line (readable on figure 3) provided between the third terminal and the second sacrificial terminal.

Regarding claim 9, as best the Examiner is able to ascertain the claimed invention, Green et al discloses on figure 3 a semiconductor die 12 comprising a Vcc bonding pad 34 coupled to the circuitry within said die 12 for supplying a first voltage to said circuitry; a secondary Vcc pad 36; a fuse 42 interconnected between the standard Vcc bonding pad 34 and the secondary Vcc pad 36, said secondary Vcc pad supplying said first voltage through said fuse 42 to the Vcc bonding pad, said fuse adapted for interrupting electrical coupling between the secondary and Vcc bonding pads when the die draws current in excess of said fuse breakdown current; a sacrificial Vcc pad 40 for receiving a first voltage; and a sacrificial metal (readable on figure 3) interconnected between the sacrificial Vcc pad and secondary Vcc pad for receiving a first voltage from the sacrificial Vcc pad and supplying said first voltage to the secondary Vcc pad.

Regarding claim 10, Green et al discloses on figure 3 the semiconductor wafer further comprises a Vss bonding pad 32 coupled to the circuitry within said die 12 for supplying a second voltage to said circuitry; a sacrificial Vss pad 38 for supplying the second voltage to the standard Vss pad; and a sacrificial metal bus (readable on figure 3) which connects the sacrificial Vss pad 38 and the standard Vss bonding pad 32.

Regarding claim 11, Green et al discloses on figure 3 the semiconductor die 12 further comprises a passivation layer which is provided with respective openings to the sacrificial Vcc and Vss pads; and Vcc and Vss sacrificial conductive busses 24, 28 formed over said passivation layer, said Vcc sacrificial conductive bus passing through an opening in said passivation layer to connect with said Vcc sacrificial pad and said

Vss sacrificial conductive bus passing through an opening in said passivation layer to connect with said Vss sacrificial pad (col. 4, lines 43-50).

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US Patent 5923047 to Chia et al discloses sacrificial bond pads for die test.

US Patent 5391892 to Devereaux et al discloses semiconductor wafers having test circuitry.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Nguyen whose telephone number is (703) 308-1269. The examiner can normally be reached on Monday-Friday, 7:30 am- 4:30 pm

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned is (703) 308-7382 for regular communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

JN
August 22, 2002

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800